DG

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8	((multiple adj board$1) or (emulation adj boards)) and (simulation or emulation) and (interconnect adj board$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 17:40
L2	198	714/741.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 17:41
L3	557	716/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 17:41
L4	1252	714/726.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 17:42
L5	91	714/717.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 17:47
L6	26	montagne-xavier.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 17:48
L9	1	(maquignon-franck.in.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 17:50
S12	2	(test$3 with (configurable adj logic adj block$1) with emulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/22 14:58
S15	6	(test$3 with configur$3 with logic with emulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/22 15:07

EAST Search History

S17	17	(test$3 with configur$3 with logic with (emulat$3 or simulat$3)) and (test$3 with FPGA$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/22 15:26
S18	14	(counter$1 with (FPGA or (configurable adj logic adj block$1))) and ((maximum adj value) with counter$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/22 18:01
S20	21	emulation same routing same logic same test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 10:18
S21	2	emulation same routing same logic same test$3 same input$1 same output$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 10:22
S22	20	emulation and (routing same logic same test$3 same input$1 same output$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 10:23
S23	5	emulation and (routing same logic same test$3 same input$1 same output$1) and FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 10:35
S30	27	(((test$3 or verif$7) with rout$3) same (emulation or simulation) same logic) and FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/23 15:21